AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of margin erasing memory cells in the testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses the same charge pump circuitry to develop both the normal erase voltage used in normal operation and the margin erase voltage used in said testing procedure

wherein a NMOS transistor affects an output of said charge pump circuitry, with its gate directly controlled by a voltage level generated only from said output of said charge pump circuitry,

wherein said voltage level at said gate of said NMOS transistor is adjusted during said margin erasing so that said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

2. (Canceled)

3. (Currently Amended) The method according to Claim 1 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing ~~series~~ serially connected voltage dropping components.

4. (Currently Amended) The method according to Claim 3 wherein said ~~series~~ serially connected voltage dropping components are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.

5. (Currently Amended) The method according to Claim 3 wherein said ~~series~~ serially connected voltage dropping components are not bypassed during development of said normal erase voltage.

6. (Original) The method according to Claim 1 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected NMOS transistors.

7. (Original) The method according to Claim 6 wherein said plurality of diode-connected NMOS transistors is not bypassed during development of said normal erase voltage.

8. (Original) The method according to Claim 1 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected PMOS transistors.

9. (Original) The method according to Claim 8 wherein said plurality of diode-connected PMOS transistors is not bypassed during development of said normal erase voltage.

10. (Original) The method according to Claim 1 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of native NMOS transistors.

11. (Original) The method according to Claim 10 wherein said plurality of native NMOS transistors is not bypassed during development of said normal erase voltage.

12. (Original) The method according to Claim 1 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diodes.

13. (Original) The method according to Claim 12 wherein said plurality of diodes is not bypassed during development of said normal erase voltage.

14. (Currently Amended) A method of margin erasing memory cells in the testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses the same internal charge pump circuit to develop both the normal erase voltage used in normal operation and the margin erase voltage used in said testing procedure;

wherein a NMOS transistor affects an output of said charge pump circuit, with its gate directly controlled by a voltage level generated only from said output of said charge pump circuit,

and wherein said voltage level at said gate of said NMOS transistor is adjusted during said margin erasing so that said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing ~~series~~ serially connected voltage dropping components wherein said voltage is reduced by m times a threshold voltage of one of said voltage dropping components where m is the number of voltage dropping components connected in ~~said series~~ the same.

15. (Currently Amended) The method according to Claim 14 wherein margin erase voltage is reduced by bypassing ~~series~~ said serially connected voltage dropping components.

16. (Currently Amended) The method according to Claim 15 wherein said ~~series~~ serially connected voltage dropping components are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.

17. (Currently Amended) The method according to Claim 15 wherein said ~~series~~ serially connected voltage dropping components are not bypassed during development of said normal erase voltage.

18. (Original) The method according to Claim 14 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected NMOS transistors.

19. (Original) The method according to Claim 18 wherein said plurality of diode-connected NMOS transistors is not bypassed during development of said normal erase voltage.

20. (Original) The method according to Claim 14 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected PMOS transistors.

21. (Original) The method according to Claim 20 wherein said plurality of diode-connected PMOS transistors is not bypassed during development of said normal erase voltage.

22. (Original) The method according to Claim 14 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced said normal erase voltage by bypassing a plurality of native NMOS transistors.

23. (Original) The method according to Claim 22 wherein said plurality of native NMOS transistors is not bypassed during development of said normal erase voltage.

24. (Original) The method according to Claim 14 wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diodes.

25. (Original) The method according to Claim 24 wherein said plurality of diodes is not bypassed during development of said normal erase voltage.

26. (Currently Amended) A flash EPROM memory device comprising:

a charge pump circuit;

a diode having a cathode and an anode wherein said cathode of said diode is connected to said flash EPROM memory device through a high voltage switch;

a plurality of series connected voltage dropping devices wherein a drain of a first of said plurality of series connected voltage dropping devices is connected to said anode of said diode wherein said charge pump circuit is connected in series with said plurality of series connected voltage dropping devices;

a NMOS transistor affects an output of said charge pump circuitry, with its gate coupled to said output of said charge pump circuit through said voltage dropping devices, wherein said voltage level at said gate of said NMOS transistor is adjusted during said margin erasing;

a bias current source connected to a source of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices wherein during normal operation of said flash EPROM memory device, said

plurality of series connected voltage dropping devices is not bypassed wherein said charge pump circuit provides a normal erase voltage and wherein during margin erasing, said plurality of series connected voltage dropping devices is bypassed wherein said charge pump circuit provides a margin erase voltage that is lower than said normal erase voltage.

27. (Original) The method according to Claim 26 wherein said series connected voltage dropping devices are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.